

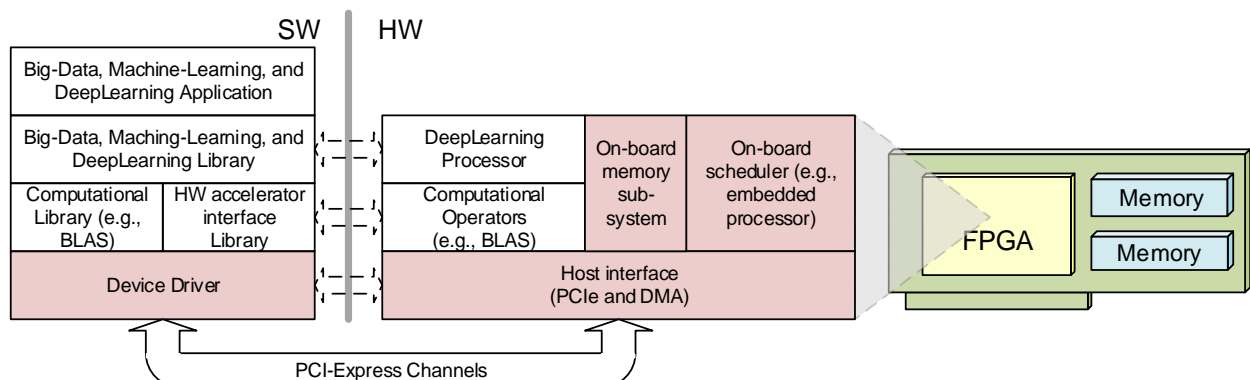
Overview

- DeepAccel-KU is an FPGA board with Xilinx Kintex UltraSCALE.
- DeepAccel-KU supports dual DDR3-72-bit SODIMM with ECC.
- DeepAccel-KU complies with PCI-Express Low Profile.
- DeepAccel-KU supports PCI-Express Gen3 with 8 lanes.
- DeepAccel-KU has SATA and SAS.

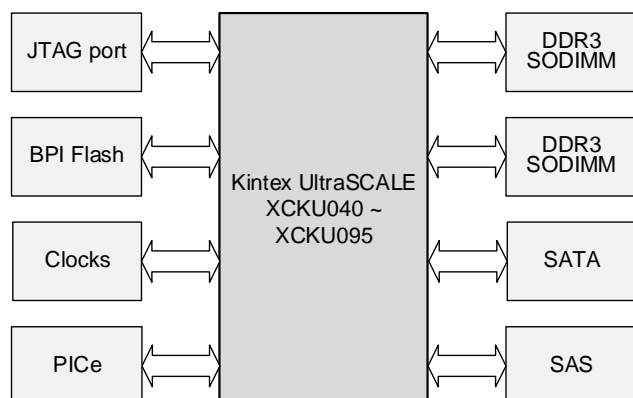


Applications

- Big-data processing
- Machine-learning
- Deep-learning
- Reconfigurable computing
- Heterogeneous computing
- Logic-simulation acceleration
- OpenCL
- Hadoop



DeepAccel-KU block diagram



Deliverables

PCI-Express Low-Profile Card
 Example design
 Linux 64-bit device driver
 Linux application programming interface

Embedded processor platform

- AHB-based
- AXI-based

DeepAccel-KU Specification

FPGA supporting		
	XCKU040 ~ 095	Xilinx Kintex UltraSCALE series
	Capacity	Logic Cells : 530K ~ 1,176K BRAM : 21.1Mb ~ 59.1Mb DSP slices : 768 ~ 4,100
Memory		
	DDR3	Two SODIMM 8GByte (x72) with ECC
	BPI FLASH	FPGA bitstream
External interfaces		
	PCI-Express	GEN3 (8GT/s per lane) 8 Lanes
	SATA	2 Channels
	SAS	4 Channels
	JTAG	FPGA configuration

• **H.Q.:** Future Design Systems Inc.
 Faculty Wing F723, KAIST Munji Campus
 193 Munji-ro, Yuseong-gu,
 Daejeon 34051, Korea
 Tel: +82-42-864-0211

Copyright © 2017~2018 by Future Design Systems Inc. All rights reserved.

Future Design is registered trademark of Future Design Systems Inc.
 The Future Design logo and DeepAccel are trademarks of Future Design Systems Inc.

All other brand or product names may be trademarks or registered trademarks of their respective holders.

Web: www.future-ds.com

E-mail: contact@future-ds.com