FUTURE Design Systems

DeepAccel-DualVU9P

Xilinx Virtex UltraScale+ with PCIe

Preliminary

Overview

- DeepAccel-DualVU9P is an FPGA board with two Xilinx Virtex UltraScale+ FPGA.
- DeepAccel-DualVU9P supports 6 channels of DDR4 Memory.
- DeepAccel-DualVU9P supports two PIC-Express Gen3 with 8 lanes.

DualVU9P Active Cooling Model

DualVU9P Passive Cooling Model

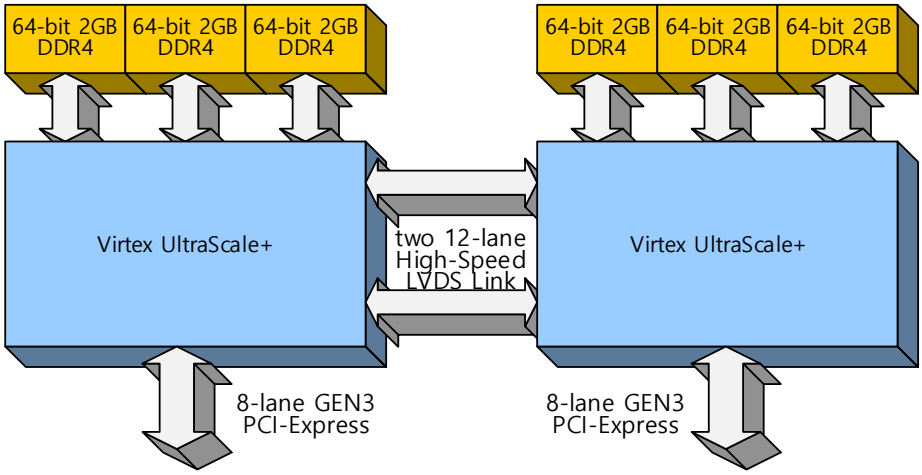
Applications

- Big-data processing
- Machine-learning
- Deep-learning
- Reconfigurable computing
- Heterogeneous computing
- Logic-simulation acceleration
- OpenCL

Deliverables

- Active cooling version
- Passive cooling version
- Linux 64-bit device driver
- Windows 64-bit device driver
- Example design

DeepAccel-DualVU9P block diagram



DeepAccel-DualVU9P Specification

FPGA supporting		
	XCVU9P	Two Xilinx Virtex UltraScale+
	Capacity	Logic Cells : 2,586K / FPGA BRAM : 75.9Mb / FPGA URAM : 270Mb / FPGA DSP slices : 6,840 / FPGA
Memory		
	DDR4	2GByte 64-bit per channel 3 channel per FPGA 6 channels per board
	BPI FLASH	FPGA bitstream
External and Chip-to-Chip interfaces		
	PCI-Express	GEN3 (8GT/s per lane) 8 Lanes per FPGA
	FPGA to FPGA	Dual 12 lane Aurora 23bit LVDS
	USB-JTAG	FPGA configuration (USB2.0 Micro-B type)

OS supporting		
	Linux	64-bit device driver • Ubuntu • CentOS
	Windows	64-bit device driver • Windows 7 • Windows 10
Power		
	300W total	• PCIe slot (75W) • 6-pin PCIe Power Connector (75W) • 8-pin PCIe Power Connector (150W)
Physical dimension		
	Active cooling	312 x 99 x 43 (mm)
	Passive cooling	312 x 99 x 43 (mm)

• **H.Q.: Future Design Systems**
Faculty Wing F723, KAIST Munji Campus
193 Munji-ro, Yuseong-gu,
Daejeon 34051, Korea
Tel: +82-42-864-0211

Web: www.future-ds.com **E-mail: contact@future-ds.com**

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